Please add the following new claims 23 and 24:

11 ~~23~~ (New). The display of claim 1 wherein said block is a nanoblock.

A3 12 ~~24~~ (New). The display of claim ~~23~~ 11 wherein said nanoblock includes an upper surface exposed when said block is mounted in said recess, said upper surface being substantially coplanar with said substrate.

REMARKS

The Applicant submitted an Information Disclosure Statement on June 29, 2001. In the present office action, the Examiner indicates that one of the three references was considered but did not check off the other two under "other documents." The Examiner is respectfully requested to complete the form so that the record reveals that the Examiner did in fact consider all three cited references.

Claim 1 has been amended to call for the block to be set within a recess. While previous dependent claim 5 called for a recess in the substrate to receive the block, this limitation was not specifically addressed in the office action.

In Figure 8, Matthies simply plugs an integrated circuit 134 onto the circuit module 702, which is in turn coupled to a display module 704. It is the display module 704 that includes the substrate 706, not the circuit module 702. The substrate must include the display elements and, again, it is clear that it is the module 704 that includes the display elements, not the circuit module 702.

Thus, Matthies fails to teach the elements of claim 1 as originally submitted. First of all, the integrated circuit chip 134 is not a block. But even if one considers the circuit 134 to be a block, there is not a block secured to each of a plurality of substrates. Instead, a single block is secured to a circuit module. No block is secured to even a single one of a plurality of substrates. Instead, the substrate that is included in 704 is not connected to the module 134.

As amended, the block must be formed into a recess in the substrate. Certainly no such structure is anywhere suggested in Matthies.

Similarly, claim 12 calls for a front plane including a plurality of emissive display elements formed on said front plane and an integrated circuit block secured to said front plane. The front plane is between the back plane and the optical integrator. In contrast, it is certainly

apparent in Figures 7 and 8 that the integrated circuit is secured to what would constitute the back plane, not the front plane. Therefore, claim 12 patentably distinguishes over the art of record.

Claim 18 distinguishes over Matthies for the reasons already discussed.

In view of these remarks, the application is now in condition for allowance and the Examiner's prompt action in accordance therewith is respectfully requested.

Respectfully submitted,

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Timothy N. Trop, Reg. No. 28,994
TROP, PRUNER & HU, P.C.
8554 Katy Freeway, Ste. 100
Houston, TX 77024
713/468-8880 [Phone]
713/468-8883 [Fax]

APPENDIX

1 (Amended). A display comprising:

a plurality of substrates, each substrate having a recess;

a plurality of display elements formed on each substrate;

an integrated circuit block [attached to] mounted in the recess on each substrate and coupled to at least one of said display elements; and

an integrator to couple said substrates to form a tiled display.

Please cancel claim 5.

Please amend claim 6 as follows:

6 (Amended). The display of claim [5] 1 wherein [said] each block and said substrate are complementarily shaped.

Please add the following new claims 23 and 24.:

23 (New). The display of claim 1 wherein said block is a nanoblock.

24 (New). The display of claim 23 wherein said nanoblock includes an upper surface exposed when said block is mounted in said recess, said upper surface being substantially coplanar with said substrate.